AMENDMENTS TO THE CLAIMS:

The following list of claims will replace all prior versions and listings of claims in the application.

LISTINGS OF CLAIMS:

1. (currently amended) An accelerated test method for testing an integrated circuit, comprising:

taking test vector data as input to said integrated circuit to produce response data as output;

using a one-way-hash function to transform said response data into a test message digest; and

verifying said test message digest against a standard message digest to determine whether said test message digest meets a predetermined requirement, wherein said standard message digest is obtained by:

simulating behavior of said integrated circuit as well as said one-way-hash function in a computer and generating said standard message digest in response to said test vector data.

2. (original) The accelerated test method of claim 1, wherein said test message digest is verified by comparing said test message digest with said standard message digest.

3. (original) The accelerated test method of claim 1, wherein said one-way-hash function is SHA-1 performed by a SHAX.

4. (original) The accelerated test method of claim 1, wherein said one-way-hash function is MD5.

5. (original) The accelerated test method of claim 1, wherein said one-way-hash function is performed by a one-way-hash hardware circuit.

6. (currently amended) The accelerated test method of claim 5, wherein said one-way-hash hardware circuit is embedded as part of [[the]] a BIST circuit in said integrated circuit.

7. (currently amended) The accelerated test method of claim 5, wherein said integrated circuit comprises a plurality of IP blocks and a plurality of one-way-hash hardware circuits are respectively embedded in corresponding IP blocks as part of [[the]] a BIST circuit in said IP blocks.

8. (original) The accelerated test method of claim 5, wherein said one-way-hash hardware circuit is implemented within automated test equipment.

9. (original) The accelerated test method of claim 5, wherein said one-way-hash function is performed by specifically designed single chip in automated test equipment.

10. (original) The accelerated test method of claim 1, wherein said one-way-hash function is performed by a microprocessor in automated test equipment.

11. (original) The accelerated test method of claim 1, wherein said one-way-hash function is performed by a DSP in automated test equipment.

12. (original) The accelerated test method of claim 1, wherein said standard message digest is obtained by:

taking said test vector data as input to a standard integrated circuit and producing a standard response data as output; and

using said one-way-hash function to transform said standard response data into said standard message digest;

wherein said standard integrated circuit is verified to be faultless before said standard message digest is generated.

Claims 13. (cancelled)

14. (original) An accelerated test system for testing an integrated circuit, comprising:

an automated test equipment for sending test vector data to said integrated circuit so that said integrated circuit produces response data in response to said test vector data and for receiving a test message digest to be verified against a standard message digest to determine whether said test message digest meets a predetermined requirement; and

a one-way-hash module for receiving said response data and performing a one-way-hash function to generate said test message digest.

15. (original) The accelerated test system of claim 14, further comprising a comparator for comparing said test message digest with said standard message digest.

16. (original) The accelerated test system of claim 14, wherein said one-way-hash module is a SHAX performing SHA-1.

17. (original) The accelerated test system of claim 14, wherein said one-way-hash module performs MD5.

18. (original) The accelerated test system of claim 14, wherein said one-way-hash module is a one-way-hash hardware circuit.

19. (original) The accelerated test system of claim 18, wherein said one-way-hash hardware circuit is embedded as part of a BIST circuit in said integrated circuit.

20. (original) The accelerated test system of claim 18, wherein said integrated circuit comprises a plurality of IP blocks and a plurality of one-way-hash hardware circuits are respectively embedded in corresponding IP blocks as part of the BIST circuit in said IP blocks.

21. (original) The accelerated test system of claim 18, wherein said one-way-hash hardware circuit is implemented within said automated test equipment.

22. (original) The accelerated test system of claim 18, wherein said one-way-hash hardware circuit is a specifically designed single chip in said automated test equipment.

23. (original) The accelerated test system of claim 14, wherein said one-way-hash module is represented by a code and programmed in a microprocessor in said automated test equipment.

24. (original) The accelerated test system of claim 14, wherein said one-way-hash function is performed by a DSP in automated test equipment.

25. (currently amended) An integrated circuit for accelerated testing, comprising:

a main module for producing response data in response to test vector data from automated test equipment; and

a plurality of IP blocks and a plurality of one-way-hash module, wherein said one-way-hash modules are used for receiving said response data and performing a one-way-hash function to generate a test message digest to be sent to said automated test equipment, and said one-way-hash modules are respectively embedded in corresponding IP blocks as part of a BIST circuit in said IP blocks, and wherein each of said IP blocks comprises a main module;

wherein said test message digest is verified against a standard message digest to determine whether said test message digest meets a predetermined requirement in said automated test equipment.

26. (original) The integrated circuit of claim 25, wherein said one-way-hash module is a SHAX performing SHA-1.

27. (original) The integrated circuit of claim 25, wherein said one-way-hash module performs MD5.

Claim 28 (cancelled)

29. (new) An accelerated test system for testing an integrated circuit, wherein said integrated circuit comprises a plurality of IP blocks, said accelerated test system comprising:

an automated test equipment for sending test vector data to said integrated circuit so that said integrated circuit produces response data in response to said test vector data and for receiving a test message digest to be verified against a standard message digest to determine whether said test message digest meets a predetermined requirement; and

a plurality of one-way-hash hardware circuits for receiving said response data and performing a one-way-hash function to generate said test message digest, wherein said one-way-hash hardware circuits are respectively embedded in corresponding IP blocks as part of a BIST circuit in said IP blocks.

30. (new) The accelerated test system of claim 29, further comprising a comparator for comparing said test message digest with said standard message digest.